IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-7 (Canceled)

8. (Currently amended) ~~An oscillator as recited in Claim 1,~~ A method as recited in Claim 17, wherein the oscillating signal is applied to a circuit that includes a circuit flip-flop, and the first and second flip-flops are substantially the same type as the circuit flip-flop.

9. (Currently amended) ~~An oscillator as recited in Claim 1,~~ A method as recited in Claim 17, wherein the oscillating signal is applied to a circuit, and the oscillator resides on the same die as the circuit.

10. (Canceled)

11. (Currently amended) ~~An oscillator as recited in Claim 1,~~ A method as recited in Claim 17, further comprising a clock buffer configured to buffer the oscillating signal.

12. (Currently amended) ~~An oscillator as recited in Claim 1,~~ A method as recited in Claim 17, wherein the oscillating signal is provided to a primary circuit via a primary circuit buffer and further comprising an oscillating signal buffer configured to buffer the oscillating signal in the same manner that the primary circuit buffer buffers the oscillating signal as provided to the primary circuit.

13. (Currently amended) ~~An oscillator as recited in Claim 1,~~ A method as recited in Claim 17, wherein the oscillating signal is sent to a field programmable gate array (FPGA).

14. (Canceled)

15. (Currently amended) ~~An oscillator as recited in Claim 1,~~ A method as recited in Claim 17, ~~wherein~~ further comprising monitoring the oscillating signal ~~is monitored~~.

16. (Currently amended) ~~An oscillator as recited in Claim 1,~~ A method as recited in Claim 17, ~~wherein~~ further comprising monitoring the oscillating signal ~~is monitored~~ and restarting the oscillator ~~is restarted~~ if it is determined that the output has ceased to oscillate.

17. (Original) A method of generating an oscillating signal, comprising:

providing the oscillating signal as a first clock input to a first flip flop;

inverting the oscillating signal and providing the inverted oscillating signal as a second clock input to a second flip flop;

using the output of the first flip flop and the output of the second flip flop to generate a combined output that alternates between a logic low level and a logic high level; and using the combined output to sustain the oscillation of the oscillating signal.

18. (Original) The method of Claim 17 further comprising providing a startup signal to generate a first pulse of the oscillating signal.

19. (Original) The method of Claim 17 further comprising buffering the combined output and providing the buffered combined output as the oscillating signal.

20. (Original) An oscillator comprising:

a first element configured to toggle a first data output according to a first transition of an oscillating signal;

a second element configured to toggle a second data output according to a second transition of the oscillating signal;

a third element configured to receive the first data output and the second data output as inputs and provide the oscillating signal as output.

21. (Original) A method of generating an oscillating signal, comprising:

toggling a first data output according to a first transition of the oscillating signal;

toggling a second data output according to a second transition of the oscillating signal;

using the first data output and the second data output to generate an alternating output that sustains the oscillation of the oscillating signal.